What Is Claimed:

1. A silicon-on-insulator integrated circuit, comprising:

(a) a handle die;

(b) a substantially continuous ~~and unbroken~~ silicide layer over said handle die,

(c) a substantially continuous ~~and unbroken~~ first dielectric layer overlying one side of said silicide layer;

(d) a device silicon layer overlying said first dielectric layer, said device silicon layer having an upper surface;

(e) a second dielectric layer on said handle die underlying the opposite side of said silicide layer; and

(f) [interconnected transistors in and at the upper surface of said device silicon layer].

2. The integrated circuit of claim 1 wherein said silicide layer comprises a diffusion barrier to impurities.

3. The integrated circuit of claim 1 further comprising:

(g) trenches extending through said device silicon layer and separating said device silicon layer into islands.

4. The integrated circuit of claim 1 wherein said device silicon layer includes doped buried layers abutting said dielectric layer.

5. The integrated circuit of claim 1 wherein said handle wafer comprises silicon and [at least one of said dielectric layers comprises diamond].

6. The integrated circuit of claim 5 wherein [both said dielectric layers comprise diamond].

7. A silicon-on insulator integrated circuit comprising:

(a) a handle die;

(b) a first dielectric layer formed on said handle die

(c) a substantially continuous ~~and unbroken~~ silicide layer formed on said first dielectric layer, said silicide layer having a controlled resistance and providing a diffusion barrier to impurities;

(d) a substantially continuous ~~and unbroken~~ second dielectric layer disposed between said silicide layer and a device silicon layer;

(e) trenches extending through said device silicon layer and silicide layer and separating said device silicon layer into islands each with an underlying continuous silicide area; and

(f) interconnected transistors in and at an upper surface of said device silicon layer.

8. The integrated circuit of claim 7 further comprising:

(g) trenches extending through at least one of said islands to said underlying silicide area, said trenches having dielectric sidewalls and containing conductive material in contact with said silicide area.

9. The integrated circuit of claim 8 wherein said islands have a thickness no greater than about 2 μm, and said conductive material is tungsten.

10. A bonded wafer integrated circuit comprising:

(a) a handle die;

(b) a homogeneous silicide layer bonded to said handle die;

(c) a device layer bonded to said silicide layer; and

(d) interconnected transistors in and at a surface of said device layer;

wherein said silicide layer comprises bonding material that differs from material in the portion of said handle die adjacent said silicide layer and which also differs from material in the portion of said device layer adjacent said silicide layer.

11. The integrated circuit of claim 10 wherein said device layer is silicon and includes doped buried layers abutting said ~~homogeneous~~ silicide layer and forming components of said transistors.

12. The integrated circuit of claim 10 wherein said bonding material in said homogeneous silicide layer is an electrical insulator and includes radiation-hardening dopants.

13. The integrated circuit of claim 10 wherein said handle die is silicon and includes a silicon dioxide portion adjacent said homogeneous silicide layer.

14. The integrated circuit of claim 10 wherein said ~~homogeneous~~ silicide layer comprises a diffusion barrier to impurities.

15. The integrated circuit of claim 10 wherein said device includes a layer of diamond adjacent said ~~homogeneous~~ silicide layer and a layer of silicon adjacent said diamond layer, said transistors being formed in and at a surface of said silicon layer.

16. The integrated circuit of claim 10 further comprising:

(e) trenches extending into said device layer and separating a semiconductor layer of said device layer into islands that isolate each of said transistors.

17. The integrated circuit of claim 16 wherein said device layer includes a diamond layer adjacent to said homogeneous silicide layer, said trenches extending to but not through said diamond layer.

18. The integrated circuit of claim 16 wherein said ~~homogeneous~~ silicide layer is conductive, said trenches extend through said silicide layer to separate said silicide layer into buried layers between said islands and said handle die, and electrical contacts extend through said device layer to said buried layers.